REMARKS

Below, the applicant's comments are preceded by related remarks of the examiner set forth in small bold font.

> **Claims 21, 33, 34, 39 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. 4,977,380 (Martin) in view of Klughart 5,546,055 (Klughart '055).**
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> **Figures 4, 5a and 5b in combination with the entire disclosure of Martin disclose an apparatus/method for providing a variable level of capacitance having a plurality of capacitors (C13, C14...), each selectable through an independent control signal (In Figures 4 and 5b of Martin. Note the signal lines individually connected to the gates of the switching elements like Q14 that control which capacitor is connected in or out of the circuit.). These independent control signals are generated by a logic circuit (Note Figure 5a that clearly shows logic elements like U6A, U6B that forms a logic circuit.). The selected capacitors of Martin clearly provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors. Martin also clearly discloses buffer-circuitry (Note Figure 5b that shows the use of buffer circuitry like U9E. Also note column 4, around line 21 that describes these elements as "buffers".). These buffers inherently isolate. Thus in the circuit of Martin these buffers decouple the plurality of capacitors from the logic circuit that clearly prevents noise in the logic circuit from affecting the plurality of capacitors. Martin however is silent on the exact composition of the capacitors and specifically the use of MOSFET capacitors.**
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> **Figure 9 of Klughart '055 discloses the use of on-chip n-depletion MOSFET load capacitors 1230 and 1232 whose source and drain are clearly connected together as is clearly illustrated. Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '055.**
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> **Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip n-depletion MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors of Martin because, as the Martin reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art recognized equivalent capacitor such as the well-known on-chip n-depletion MOSFET capacitors as recited by Klughart '055.**
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> **...**
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> **Claims 21, 22, 29, 30, 39-42 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke in view of Ochiai et al. US 4,851,792 (Ochiai), Klughart '055 and Horn "Basic Electronics Theory" 4th Edition pp 377-378, pp 418-426 and pp 454-465.**
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> **The oscillator circuit of Clarke includes a capacitor circuit that includes a plurality of on-chip capacitors C1 -C6. Each of these capacitors is independently selectable by a control signal D0-D5. The amount of the capacitance is clearly a function of how many capacitors are The connected. voltage signal V_{bias} is**

considered by Clarke to be a bias voltage signal and it is applied to the capacitors Cl-C6 via a resistor element 33. Clarke is silent on the composition of the on-chip capacitors. Clarke is also silent on using buffer circuitry to decouple the transmission gate switches from the set of memory registers. Clarke is silent on the use of a filtered power supply for the bias source of the capacitors.

...

Figure 8(a) of Ochiai discloses a biasing arrangement for the capacitors of an oscillator and is configured such that the bias voltage VB of the capacitor 14 "remains constant" (See column 5 around line 61 of Ochiai). This as recognized by Ochiai allows for the oscillation frequency to remain constant. It is conventionally known that changes of bias to a MOS type capacitor including MOSFET based MOS capacitors will cause changes in its capacitance much like a pin arrangement. It is the teaching of Clarke to have capacitors Cl-C6 to be capacitors having discrete i.e. non-changing values. Clarke obtains the change in capacitance by switching these capacitors of discrete values in and out of the circuit. Clarke shows and describes no means by which the individual capacitances of these capacitors are changed.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the oscillator arrangement of Clarke and Klughart '055 with a bias arrangement that keeps the necessary bias voltage of the capacitor elements constant so as to prevent the individual capacitance elements from varying in capacitance and thus preventing an undesirable drift in oscillator frequency as taught by Ochiai.

Horn teaches that buffers are used to ensure that the output drive is sufficient to drive the devices on the output thereof.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a buffers between the transmission gate switches and the memory registers so as to insure that there is sufficient drive for the transmission gate switches as taught by Horn.

Clarke is likewise silent on the use of filtered power signals to power the buffer circuitry. Buffer circuitry requires a power supply as is well known in the art so that it can provide the sufficient drive as noted above. Horn teaches that it is commonplace to utilize filtered power supplies, in particular note pages 456 and 460 to power electronic devices. This as Horn recognizes reduces "ripple", i.e. noise, or voltage fluctuations that then in turn causes less vacillations in the devices powered by such power supplies.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the filtered power supply made obvious above to power the buffers made obvious above so as to reduce the introduction of noise in the system as is taught by Horn.

Claims 21, 22, 31, 32, 39, 40-42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke 6,337,604 (Clarke) in view Ochiai et al. US 4,851,792 (Ochiai), Klughart US 5,801,411 (Klughart '411)and Horn "Basic Electronics Theory" 4th Edition pp 377-378, pp 418-426 and pp 454-465.

...

Figure 9b of Klughart '411 discloses the use of on-chip p-enhancement MOSFET capacitor 32 whose source and drain are clearly connected together as "common" i.e. conventional (See column 7, around line 18). Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to

> **ground in Klughart '411.**
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> ...
>
> **Claims 21, 31, 34, 39 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. 4,977,380 (Martin) in view of Klughart 5,801,411 (Klughart '411).**
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> ...

The references do not disclose or suggest, and would not have made obvious, "a low pass filter connected to a DC power supply to generate a bias voltage to bias the drains and sources of the MOSFET capacitors and to power the buffer circuitry," as recited in amended claim 21, for at least two independent reasons, any of which would be sufficient to overcome the examiner's rejection.

<u>First reason for why claim 21 would not have been obvious</u>:

The combination of Martin and Klughart '055, or the combination of Martin and Klughart '411, would not have made obvious "a bias voltage to bias the drains and sources of the MOSFET capacitors."

Neither Martin nor Klughart '055 discloses or suggests "a bias voltage to bias the drains and sources of the MOSFET capacitors." Martin merely discloses an electrically tuned power oscillator (ETPO) having capacitors, each connected in series with an FET switch that determines whether the capacitor is coupled to the ETPO (see Fig. 4). Klughart '055 merely discloses drain-source connected N-depletion MOSFET capacitors 1230 and 1232 that are coupled to a crystal resonator 1228, in which the drains and sources of the N-depletion MOSFETs 1230 and 1232 are connected to ground (see FIG. 9). If a drain-source connected MOSFET of Klughart '055 were used with an FET switch of Martin, the drain and source of each MOSFET capacitor could be connected to either the drain of the FET switch, or to the transformer T2 or T3 (see Fig. 4 of Martin).

If the drains and sources of the MOSFETs were connected to the drain of the FET switches, it would not have been obvious to have "a bias voltage to bias the drains and sources of

the MOSFET capacitors," because doing so would cause electric current to flow through the FET switch and resistor R1 (see Fig. 4 of Martin) to ground, wasting electric power. If the drains and sources of the MOSFETs were connected to the transformer T2 or T3, it would also not have been obvious to have "a bias voltage to bias the drains and sources of the MOSFET capacitors," because doing so would keep the voltage at the transformer at a constant level and prevent or reduce oscillation of the ceramic transducer X1.

Similar to the reasons above, the combination of Martin and Klughart '411 would not have made obvious "a bias voltage to bias the drains and sources of the MOSFET capacitors."

For similar reasons, the combination of Clarke, Klughart '055, Ochiai, and Horn, or the combination of Clarke, Klughart '411, Ochiai, and Horn, would not have made obvious "a bias voltage to bias the drains and sources of the MOSFET capacitors."

None of the above references, individually or in combination, discloses or suggests "a bias voltage to bias the drains and sources of the MOSFET capacitors." Ochiai merely discloses a floating gate MOS variable capacitor, and Horn merely discloses a low pass filter. Clarke merely shows capacitors, each having two ends, in which one end is connected to ground and the other end is connected to a Vbias voltage through a resistor (see only figure of Clarke). Klughart '055 merely discloses drain-source connected N-depletion MOSFETs 1230 and 1232 in which the drains and sources are connected to ground (see FIG. 9). Klughart '411 merely discloses drain-source connected P-type MOSFET capacitors in which the drains and sources are connected to ground. Klughart '411 also discloses applying a bias voltage to the gate terminal of the capacitor (col. 1, lines 57-58).

The combination of Clarke and Klughart '055, or the combination of Clarke and Klughart '411, might have suggested to a person skilled in the art to connect the drains and sources of the MOSFET capacitors to ground and apply the Vbias voltage to the gates of the MOSFET capacitors. There would have been no suggestion or motivation to use a bias voltage to bias the drains and sources of the MOSFET capacitors, as required by claim 21.

<u>Second reason</u> <u>for why claim 21 would not have been obvious</u>:

The combination of cited references would not have made obvious "a low pass filter connected to a DC power supply to generate a bias voltage to bias the drains and sources of the MOSFET capacitors" (emphasis added), as recited in amended claim 21.

Martin, Clarke, Ochiai, Klughart '055, and Klughart '411 do not disclose or suggest the use of a low pass filter to generate a bias voltage. Clarke merely shows a Vbias voltage applied to the capacitors through a resistor (see only figure of Clarke). Ochiai merely shows a bias voltage generated by a constant voltage circuit and a voltage divider (see FIG. 8a). Horn merely discloses a low pass filter to reduce ripples in a voltage signal generated by a resistor-diode combination that rectifies an AC voltage (see page 456). Klughart '055 and '411 merely disclose drain-source connected MOSFETs in which the drains and sources are connected to ground (see FIG. 9).

The examiner appears to take the position that because Horn teaches the use of a low pass filter to generate a voltage signal with less ripple, and Clarke discloses a bias voltage without saying how the bias voltage is generated, it would have been obvious to use the low pass filter of Horn to generate the bias voltage of Clarke. The applicant disagrees.

The prior art must suggest the desirability of the claimed invention. See MPEP 2143.01. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggest the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990).

In Horn, the output of the resistor-diode combination swings from 0V to the peak amplitude of the AC voltage, and thus there is a need for a low pass filter to reduce the ripples. Clarke has a DC voltage power supply Vcc. Ochiai teaches the use of a voltage divider to generate a bias voltage. There is no suggestion or motivation to use the low pass filter of Horn in the oscillator circuit of Clarke or Ochiai.

Horn also teaches the use of a voltage divider to generate a smaller voltage from a voltage supply. Given the disclosure of a DC voltage power supply in Clarke, and the use of a

voltage divider in Ochiai, the combination of Clarke, Ochiai, and Horn would have suggested the use of a voltage divider to generate a bias voltage.

The invention of claim 21 includes the recognition that the drain-source connected MOSFET capacitors may be used in an environment in which noise generated by other components may be coupled to the capacitors through the power supply signal line and adversely affect the operation of the circuit using the capacitors. Thus, rather than using a voltage divider to derive the bias voltage from a DC power supply, it is advantageous to use a low pass filter connected to the DC power supply to generate the bias voltage. Neither Ochiai, Clarke, Klughart '055, Klughart' 411, nor Horn discloses or suggests that noise generated by other components may be coupled to the capacitors through the power supply signal line and adversely affect the operation of the circuit using the capacitors.

Claim 39 is patentable for at least the same reasons as claim 21.

> **Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. 4,977,380 (Martin) in view of Morand et al. 6,734,483 (Morand).**
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> **Figures 4, 5a and 5b in combination with the entire disclosure of Martin disclose an apparatus/method for providing a variable level of capacitance having a plurality of capacitors (C13, C14...), each selectable through an independent control signal (In Figures 4 and 5b of Martin. Note the signal lines individually connected to the gates of the switching elements like Q14 that control which capacitor is connected in or out of the circuit.). These independent control signals are generated by a logic circuit (Note Figure 5a that clearly shows logic elements like U6A, U6B that forms a logic circuit.). The selected capacitors of Martin clearly provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors. Martin also clearly discloses buffer circuitry (Note Figure 5b that shows the use of buffer circuitry like U9E. Also note column 4, around line 21 that describes these elements as "buffers".). These buffers inherently isolate. Thus in the circuit of Martin these buffers decouple the plurality of capacitors from the logic circuit that clearly prevents noise in the logic circuit from affecting the plurality of capacitors. Martin however is silent on the integration of the circuit and exact composition of the capacitors and specifically the use of on-chip metal or on-chip poly capacitors.**
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> **To integrate a circuit is well known to save space and make for a more reliable structure. This is further supported by Morand that teaches the use for poly capacitors to be included in an integrated circuit. See column 1 around line 19 of Morand.**
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> **Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip poly capacitors in place of the generic capacitors of Martin because, as the Martin reference is silent as to**

> **the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known poly capacitor as recited by Morand. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have integrated the circuit of Martin so as to save space and make for a more reliable structure as is well known in the art and as taught by Morand.**
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> ...
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> **Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin and Morand as applied to claim 35 above, and further in view of Early et al. 5,391,999 (Early).**
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> **As noted above Martin utilizes MOSFETs for the switching elements that switch in and out the capacitors that make up the variable capacitor of Martin. Martin is silent on the use of "transmission gates" for the switching elements.**
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> **Early discloses that the shown N-channel transistors (MOSFETs) and the shown Transmission gates are switching elements and that many different elements may be substituted therefore (See the paragraph that begins around line 37). Thus Early clearly recognizes the art recognized equivalence of these elements as well as the equivalence of these elements with many other forms of switching devices.**
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> **Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted transmission gates for the MOSFETs of Martin. One of ordinary skill in the art would have been motivated to make the substitution for these are art recognized equivalent forms of switches that can be used in place of one another as recognized and taught by Early.**

Martin does not disclose or suggest "buffer circuitry for decoupling the transmission gates from the logic circuit to prevent noise in the logic circuit from affecting the selected capacitors," in which "the logic circuit ha[s] sufficient driving power to switch the transmission gates," as recited in amended claim 35. In Martin, the drivers U9A to U9D (see Fig. 5B) are used to drive the switching elements (col. 4, lines 23-25), so the drivers U9A to U9D in Martin would be part of the "logic circuit' of claim 35. Martin does not disclose or suggest using buffer circuitry to decouple transmission gates from a logic circuit when the logic circuit already has sufficient driving power to switch the transmission gates.

What is missing in Martin is not disclosed or suggested by Morand, which merely discloses different types of capacitors.

What is missing in Martin and Morand is also not disclosed or suggested by Early, which merely discloses transmission gates.

The invention of claim 35 includes the recognition noise from the logic circuit may be coupled to the capacitors through the transmission gates and adversely affect the operation of the

capacitors. Thus, buffer circuitry is provided, not to drive the transmission gates, but to "decoupl[e] the transmission gates from the logic circuit to prevent noise in the logic circuit from affecting the selected capacitors." Neither Ochiai, Clarke, Klughart '055, Klughart' 411, nor Horn discloses or suggests that noise from a logic circuit may be coupled to the capacitors through transmission gates and adversely affect the operation of the capacitors.

The dependent claims are patentable for at least the same reasons as the claims on which they depend.

Cancelled and amended claims have been cancelled and amended, respectively, without prejudice. The applicant reserves the right to pursue those claims in a continuing application.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

No fee is due. Please apply any charges or credits to deposit account 06-1050, referencing attorney docket 10559-650003.

Respectfully submitted,

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** See attached document certifying that Rex Huang has limited recognition to practice before the U.S. Patent and Trademark Office under 37 CFR § 10.9(b).*